AMENDMENTS TO THE CLAIMS

1. (Previously presented) A method of controlling a power supply comprising:

reading a digital signal on a digital data bus, said digital signal including information relating to an anticipated change in power demand;

generating a control signal based on said information;

feeding said control signal forward to a power supply; and

modifying a power output of said power supply to a load in response to said control signal, wherein said power supply further comprises a plurality of charge pump circuits and a respective plurality of clock generation circuits, each of said clock circuits operatively connected to, and adapted to drive, a respective charge pump circuit,

wherein said act of modifying said power output further comprises activating more than one of said plurality of charge pump circuits in response to said control signal.

2. (Cancelled).

3. (Previously presented) A method of controlling a power supply as defined in claim 1 further comprising:

enabling more than one of said plurality of clock circuits and thereby driving said respective charge pump circuit.

4. (Original) A method of controlling a power supply as defined in claim 1 wherein said digital data bus is configured as a parallel data bus.

5. (Original) A method of controlling a power supply as defined in claim 1 wherein said control signal is a digital signal.

6. (Original) A method of controlling a power supply as defined in claim 1 wherein said control signal is an analog signal.

7. (Original) A method of controlling a power supply as defined in claim 6 wherein said analog signal further comprises a voltage signal having a magnitude proportional to a multiple of data bits of a data word on said data bus having a particular state.

8. (Original) A method of controlling a power supply as defined in claim 7 wherein said multiple of data bits comprises four data bits.

9. (Original) A method of controlling a power supply as defined in claim 7 further comprising:

generating said voltage signal by flowing an electrical current through a voltage divider circuit.

10. (Previously presented) A method of controlling a power supply as defined in claim 9 wherein said voltage divider circuit further comprises a plurality of resistors shunted by a respective plurality of transistors, each transistor being responsive to a respective data line of said data bus.

11. (Previously presented) A method of controlling a power supply as defined in claim 1 wherein said load comprises a digital memory circuit.

12. (Original) A method of controlling a power supply as defined in claim 11 wherein said digital memory circuit further comprises a flash memory circuit.

13. (Original) A method of controlling a power supply as defined in claim 12 further comprising:

storing a portion of said digital data signal as a data word in said flash memory circuit.

14. (Cancelled).

15. (Previously presented) A method of controlling a power supply comprising:

producing an analog signal related to a number of bits having a particular logic state in a digital signal, said analog signal being independent of an output of said power supply; and

setting an output of said power supply to a particular level in response to said analog signal, wherein said power supply comprises a plurality of subcircuits and said setting an output of a power supply comprises activating more than one of said subcircuits, said subcircuits each including a respective charge pump circuit and

wherein said activating said subcircuits further comprises, for each subcircuit, enabling a clock circuit connected to drive a respective charge pump circuit.

16. (Cancelled)

17. (Cancelled)

18-23. (Cancelled).

24. (Currently amended) A method of controlling a power supply comprising:

sensing a number of bits in a particular logic state in a particular digital communication; and

adapting said power supply to supply a particular level of current, said level of current being proportional to said number of bits by switchingly connecting a plurality of power supply portions to a load circuit,

each power supply portion comprising a charge pump circuit and a respective clock generation circuit, each of said clock circuits operatively connected to, and adapted to drive, a respective charge pump circuit,

wherein said act of supplying a particular level of current comprises activating more than one of said plurality of power supply portions.

25-35. (Cancelled).

36. (Previously presented) A power supply apparatus comprising:

a plurality of charge pump circuits;

a control circuit having a data input and at least one control output, said at least one control output being operatively connected to more than one of said plurality of charge pump circuits, said control circuit adapted to activate more than one of said plurality of charge pump circuits in response to a received signal on said data input containing information relating to an anticipated change in power demand.

37. (Previously presented) A power supply apparatus comprising:

a plurality of charge pump circuits;

an input bus having a plurality of input lines;

a control circuit connected to said input bus, said control circuit adapted to provide a particular plurality of output signals in response to a number of bits of a predetermined logic value in an input signal received on said input lines containing information relating to an anticipated change in power demand;

a plurality of groups of outputs of said control circuit, each group of outputs being operatively connected to a respective charge pump circuit, said outputs being adapted to transmit said plurality of output signals to said plurality of charge pumps by their respective groups, whereby said plurality of charge pumps are each activated or deactivated in response to said respective plurality of groups of output signals.

38. (Cancelled).

39. (Currently amended) A power supply controller comprising:

a plurality of data bus inputs;

a plurality of outputs;

a sensing circuit adapted to activate one or more of said plurality of outputs in response to a corresponding pattern of data bus signals detected on said plurality of data bus inputs and

a plurality of charge pump circuits connected to one of said plurality of outputs, said plurality of charge pump circuits being adapted to modify said power output by activating more than one of said plurality of charge pump circuits.

40. (Cancelled).

41. (Previously presented) A processing system comprising:

a microprocessor;

a data bus, said data bus connected to said microprocessor;

an electronic memory device having a plurality of data bus inputs connected to said data bus, said electronic memory device including a power supply controller having a plurality of outputs and a sensing circuit adapted to activate more than one of the plurality of outputs in response to a pattern of data bus signals detected on said plurality of data bus inputs and

a plurality of charge pump circuits each operatively connected to a respective output.

42. (Cancelled).

43. (Previously presented) A microprocessor integrated circuit comprising:

a processing portion;

a memory portion connected to said processing portion by a data bus portion, said memory portion including a power supply and power supply controller, said power supply controller having a plurality of data bus inputs connected to said data bus portion, an output connected to said power supply, and a sensing circuit adapted to activate or deactivate said output in response to a corresponding pattern of data bus signals detected on said plurality of data bus inputs; and

a plurality of charge pump circuits responsive to said output, said output activating more than one of said plurality of charge pump circuits responsive to said sensing circuit.